WHAT IS CLAIMED IS:

1. A method of detecting multiple data bit errors in physically adjacent data bits in a memory boundary having a parity bit, comprising the steps of: activating each of a line of a memory boundary in a memory array having the parity bit; and, directing physically adjacent data bits in an activated line to two or more parity checking devices so that two or more physically adjacent data bits are not forwarded to the same one of the parity checking devices.

2. The method recited in claim 1 wherein multiple data bit errors can be determined in physically adjacent data bits by error logic control.

3. The method recited in claim 1 wherein directing includes at least a pair of parity checking devices for detecting double-bit errors in physically adjacent data bits wherein alternating data bits are directed to alternating parity checking devices.

4. An apparatus for use in detecting multiple data bit errors in physically adjacent data bits in a memory boundary of a memory array in response to data fetching, comprising: a memory array including a memory boundary having a parity bit in an activatable line; and, two or more parity checking devices for checking parity coupled to the memory array in a manner so that two or more physically adjacent data bits are not forwarded to the same one of the parity charity devices.

5. The apparatus recited in claim 4 wherein double-bit errors in physically adjacent data bits can be determined by error logic control.

6. The apparatus recited in claim 4 wherein double-bit errors are determined by a pair of parity checking devices for detecting double-bit errors in physically adjacent data bits wherein alternating data bits are directed to alternating ones of the pair of parity checking devices.

7. The apparatus recited in claim 4 wherein the memory array is constructed on a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS).

8. The apparatus recited in claim 4 wherein the memory array is constructed on bulk silicon.